



Features:

- Isolated mounting base 3000V~
- Pressure contact technology with increased power cycling capability
- Space and weight saving

Typical Applications

- AC/DC Motor drives
- Various rectifiers
- DC supply for PWM inverter

V _{DSM} , V _{RSM}	V _{DRM} , V _{RRM}	Type & Outline
2100V	2000V	MFx135-20-216F3/216F3B
2300V	2200V	MFx135-22-216F3/216F3B
2600V	2500V	MFx135-25-216F3/216F3B

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T _j (°C)	VALUE			UNIT
				Min	Type	Max	
I _{T(AV)}	Mean on-state current	180° half sine wave 50Hz Single side cooled, T _c =85°C	125			135	A
I _{T(RMS)}	RMS on-state current					212	A
I _{DRM} I _{RRM}	Repetitive peak current	at V _{DRM} at V _{RRM}	125			20	mA
I _{TSM}	Surge on-state current	10ms half sine wave	125			3.6	kA
I ² t	I ² t for fusing coordination	V _R =60%V _{RRM}				65	A ² s*10 ³
V _{TO}	Threshold voltage		125			0.85	V
r _T	On-state slope resistance					1.91	mΩ
V _{TM}	Peak on-state voltage	I _{TM} =410A	25			1.96	V
dv/dt	Critical rate of rise of off-state voltage	V _{DM} =67%V _{DRM}	125			800	V/μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A t _r ≤ 0.5μs Repetitive	125			100	A/μs
I _{GT}	Gate trigger current	V _A =12V, I _A =1A	25	30		150	mA
V _{GT}	Gate trigger voltage			0.7		2.5	V
I _H	Holding current			10		200	mA
V _{GD}	Non-trigger gate voltage	V _{DM} =67%V _{DRM}	125	0.2			V
R _{th(j-c)}	Thermal resistance Junction to case	Single side cooled per chip				0.20	°C /W
R _{th(c-h)}	Thermal resistance case to heat sink	Single side cooled per chip				0.08	°C /W
V _{iso}	Isolation voltage	50Hz, R.M.S, t=1min, I _{iso} :1mA(MAX)		3000			V
F _m	Terminal connection torque (M6)				6.0		N·m
	Mounting torque (M6)				6.0		N·m
T _{vj}	Junction temperature			-40		125	°C
T _{stg}	Stored temperature			-40		125	°C
W _t	Weight				320		g
Outline	216F3、216F3B						

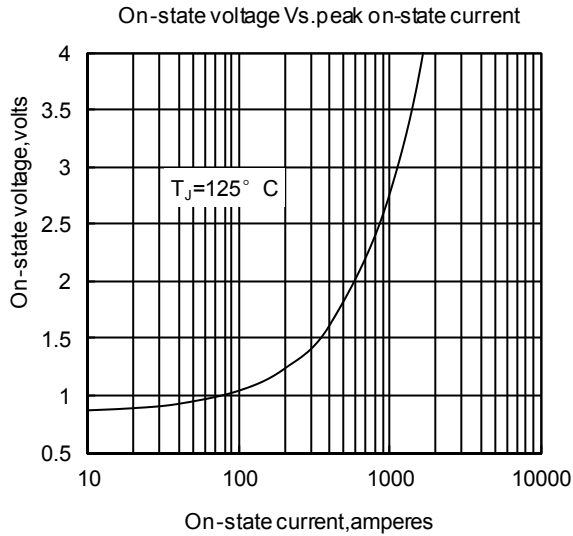


Fig. 1

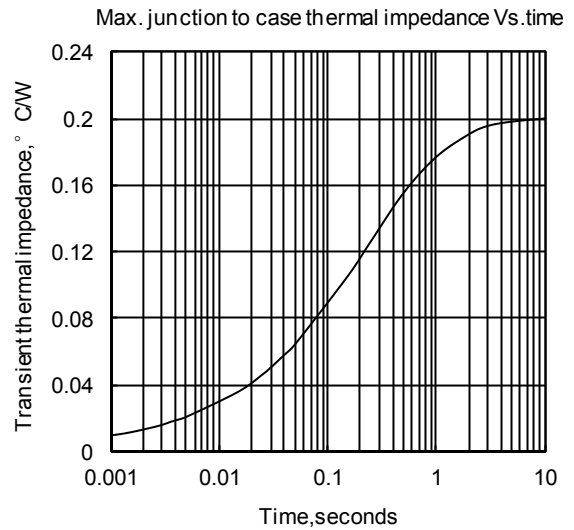


Fig. 2

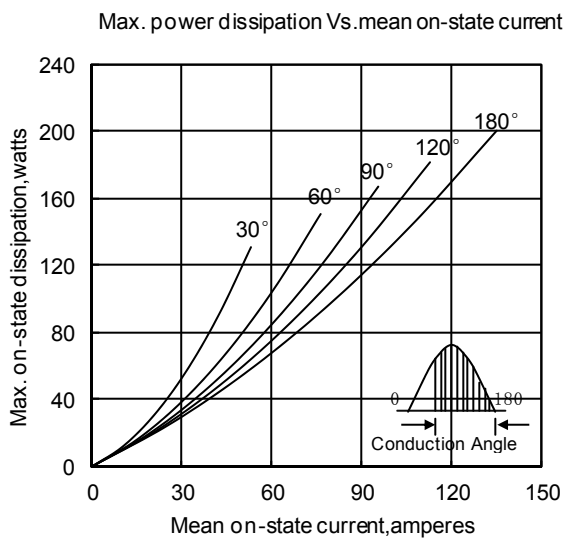


Fig. 3

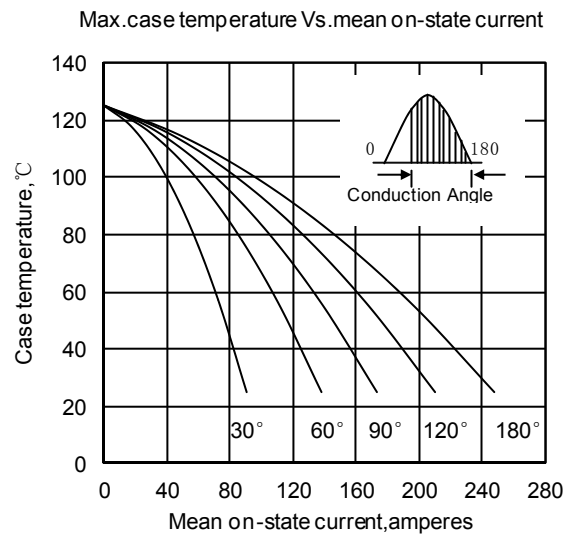


Fig. 4

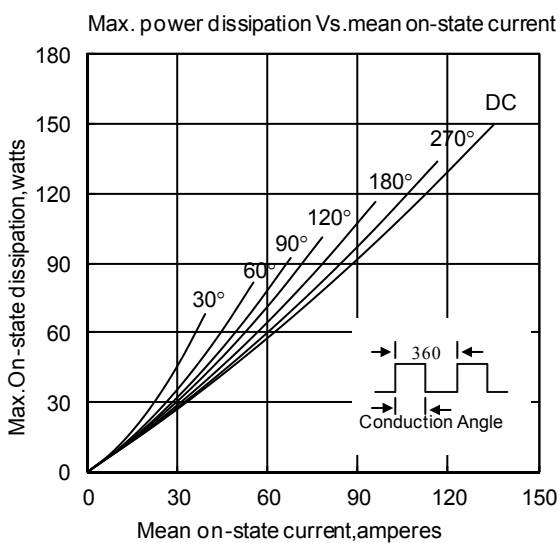


Fig. 5

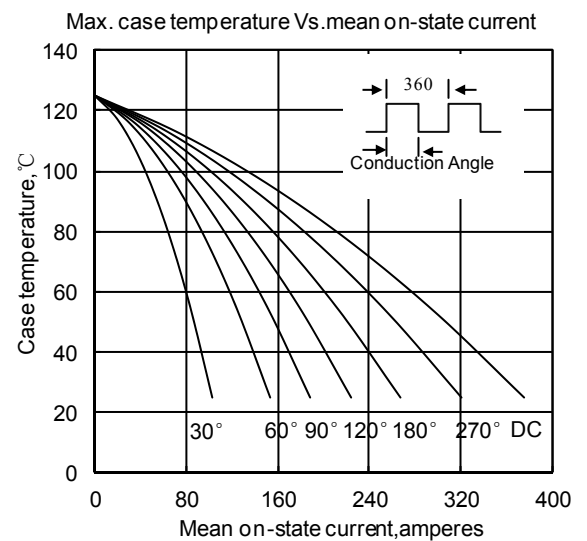


Fig. 6

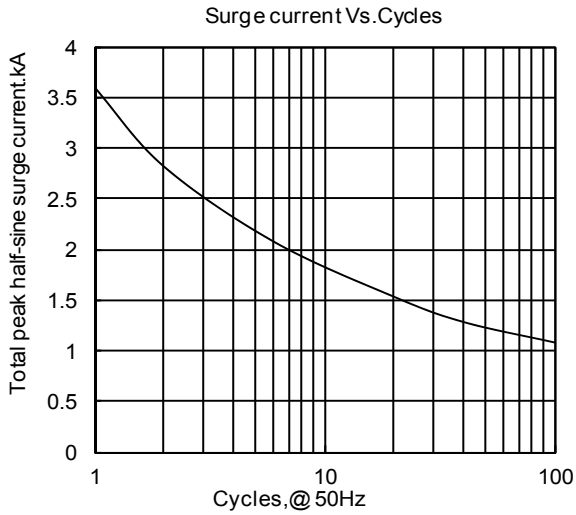


Fig. 7

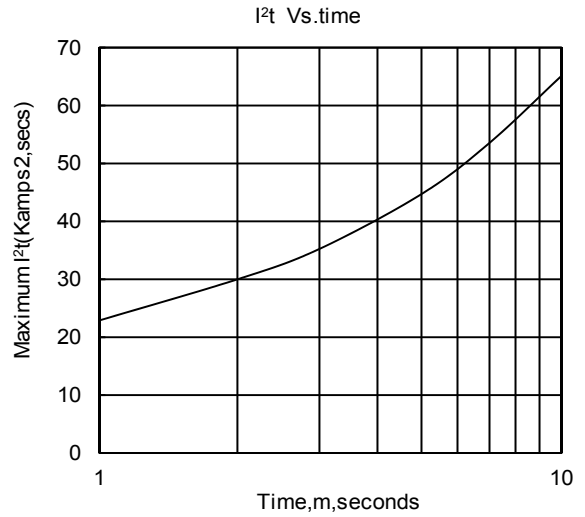


Fig. 8

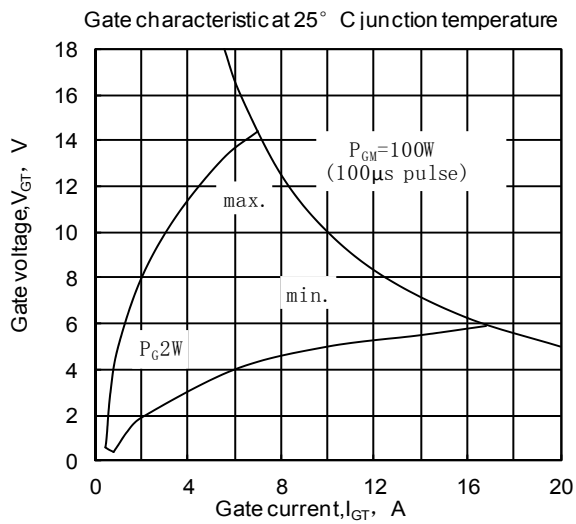


Fig. 9

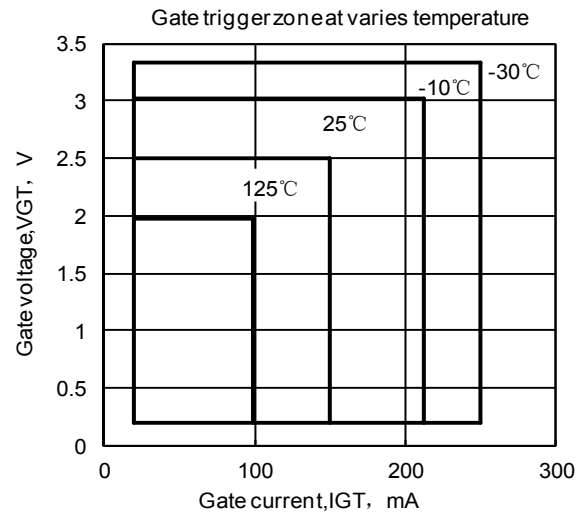
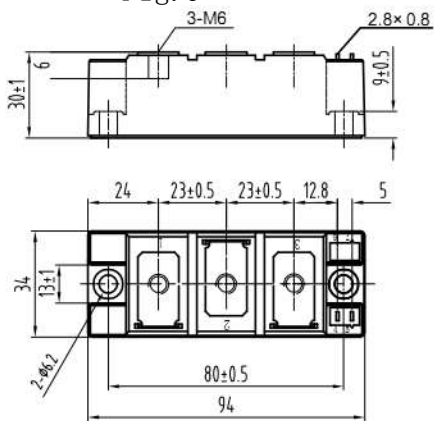


Fig. 10

Outline:



216F3: 4 is Gate



216F3B: 5 is Gate

