Features：

- Isolated mounting base 3000V~
- Pressure contact technology with Increased power cycling capability
- Space and weight saving

Typical Applications

- AC/DC Motor drives
- Various rectifiers
- DC supply for PWM inverter

V_{DSM},V_{RSM}	V_{DRM},V_{RRM}	Type & Outline
2100V	2000V	MFx26-20-215F3
2300V	2200V	MFx26-22-215F3
2600V	2500V	MFx26-25-215F3

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled, T_c=85°C	125			26	A
$I_{T(RMS)}$	RMS on-state current					41	A
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			10	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=60%V_{RRM}	125			0.65	kA
I^2t	I^2t for fusing coordination					2.10	A^2s*10^3
V_{TO}	Threshold voltage		125			0.85	V
r_T	On-state slope resistance					9.68	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=80A	25			2.8	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=67%V_{DRM}	125			800	V/μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A t_r≤0.5μs Repetitive	125			50	A/μs
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	30		150	mA
V_{GT}	Gate trigger voltage			0.7		2.5	V
I_H	Holding current			10		200	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}	125	0.2			V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.95	°C /W
$R_{th(c-h)}$	Thermal resistance case to heat sink	Single side cooled per chip				0.20	°C /W
V_{iso}	Isolation voltage	50Hz,R.M.S,t=1min,Iiso:1mA(MAX)		3000			V
F_m	Terminal connection torque (M5)				4.0		N·m
	Mounting torque (M6)				6.0		N·m
T_{vj}	Junction temperature			-40		125	°C
T_{stg}	Stored temperature			-40		125	°C
W_t	Weight				120		g
Outline	215F3						

On-state voltage Vs.peak on-state current

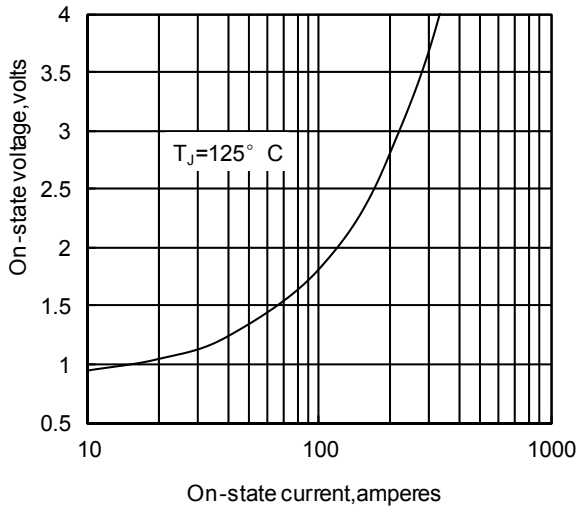


Fig1

Max. junction to case thermal impedance Vs.time

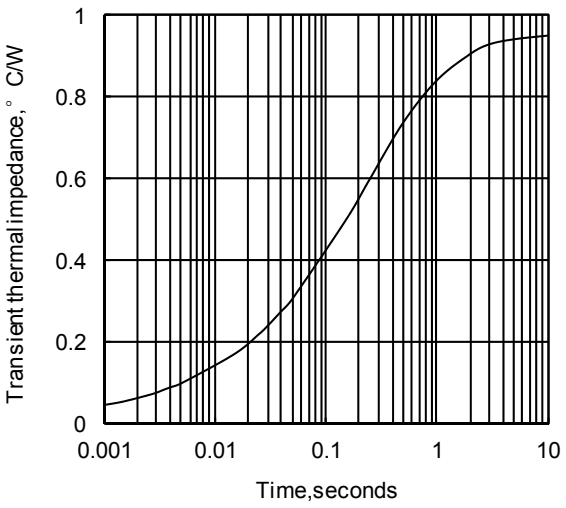


Fig2

Max. power dissipation Vs.mean on-state current

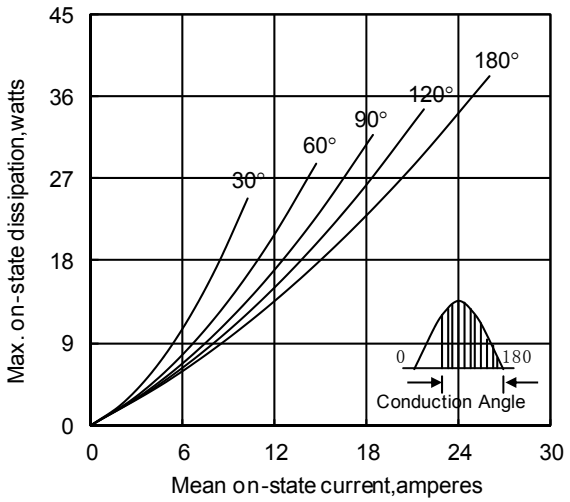


Fig3

Max.case temperature Vs.mean on-state current

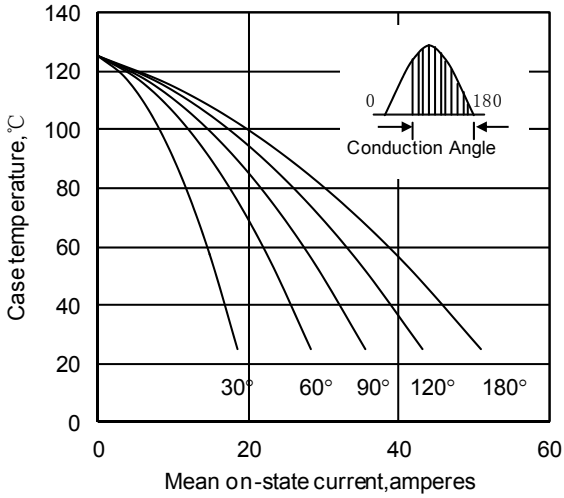


Fig4

Max. power dissipation Vs.mean on-state current

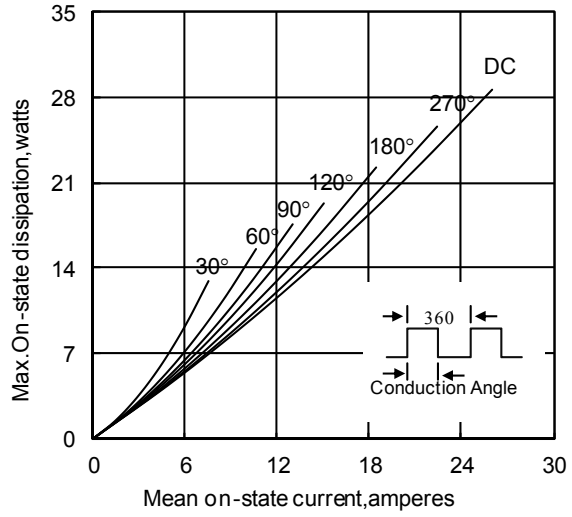


Fig5

Max. case temperature Vs.mean on-state current

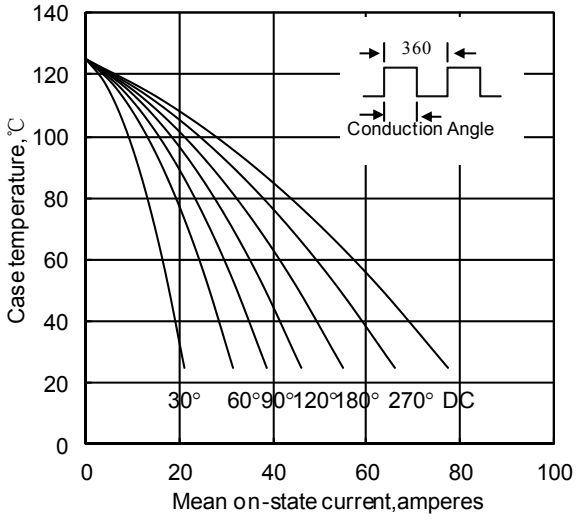


Fig6

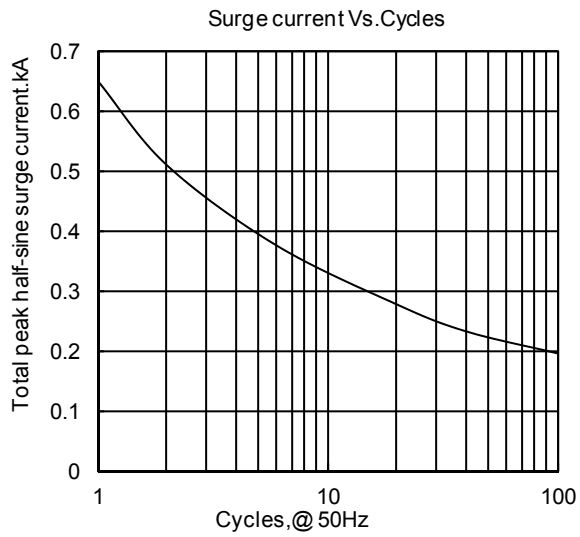


Fig7

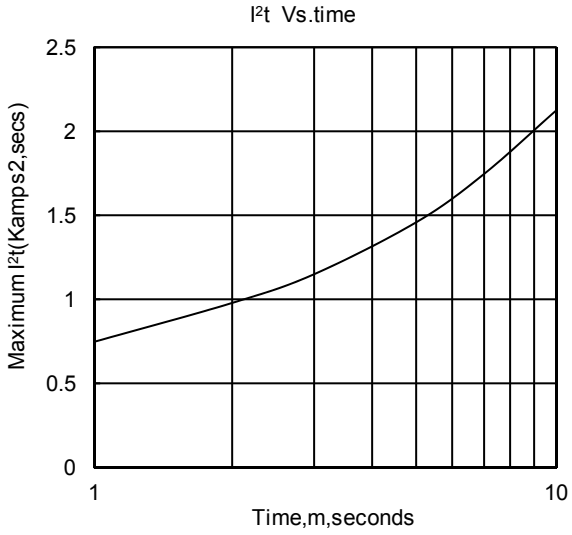


Fig8

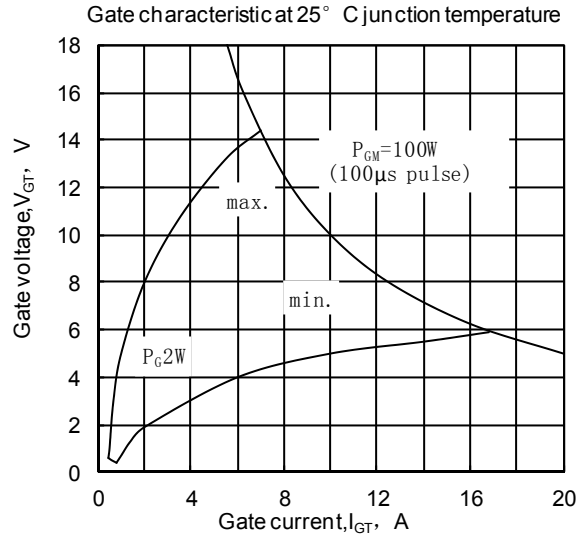


Fig9

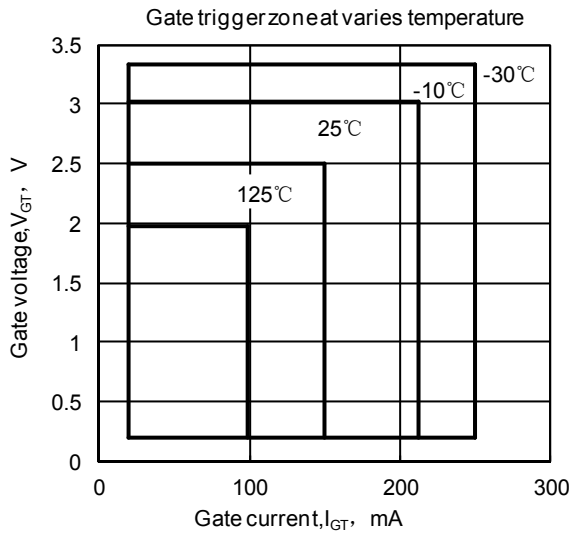
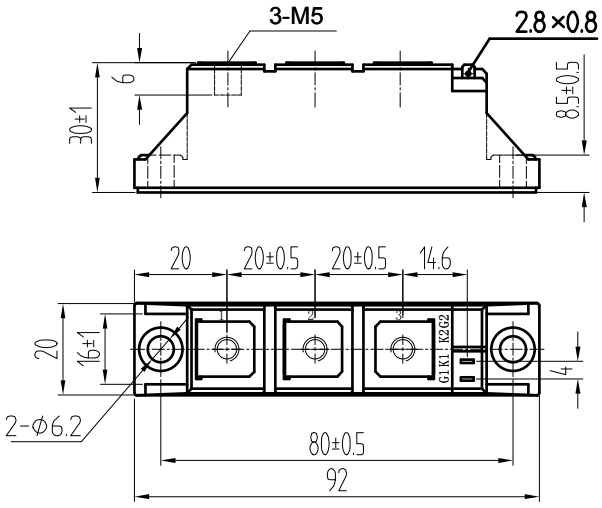
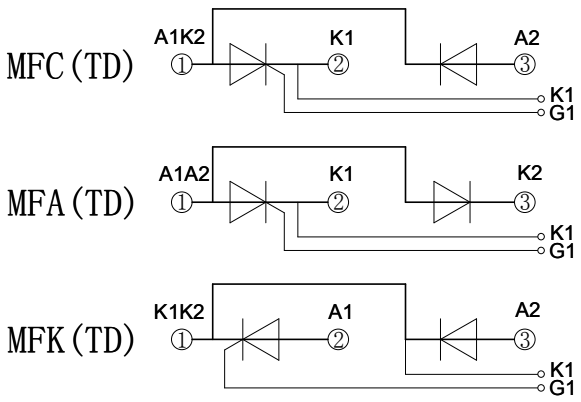


Fig10

Outline: